

Low Drain bias operation of 0.1 μ m to 0.4 μ m gate length pseudomorphic Al_{0.22}Ga_{0.78}As/In_{0.2}Ga_{0.8}As/GaAs HEMTs at cryogenic temperature

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Abstract

We investigate in this paper the combined effect of self heating and trapping centers in short gate HEMTs versus temperature. We point out the favorable transport condition at low drain bias, the limit of improvements of HF characteristics for the smallest devices, and the range of biases needed to avoid the main degradation at low temperature due to the deep levels in AlGaAs layer.

Introduction

There is a rising interest in low voltage and also in low temperature operation of HEMTs related to emerging communications. We investigate these aspects in Al_{0.22}Ga_{0.78}As/In_{0.2}Ga_{0.8}As/GaAs δ -doped ($4 \cdot 10^{12} \text{cm}^{-2}$) single-recessed PM-HEMTs (*). The technological HEMT structure is given in Fig.1. There is a 12 nm thick InGaAs strained channel a 3nm n.i.d spacer and the total gate to channel distance is 15nm. The gate lengths are 0.4 μ m, 0.3 μ m, 0.2 μ m, and 0.1 μ m.

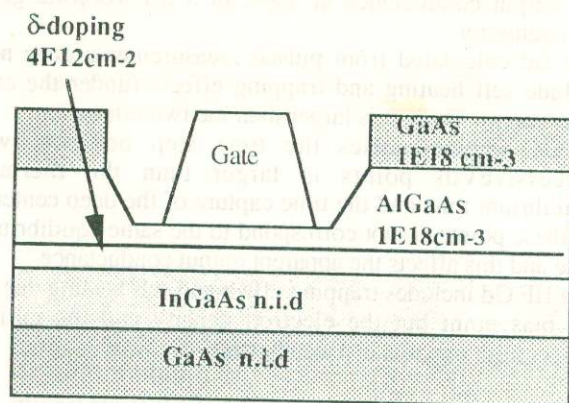


Fig. 1 : Schematic structure of pseudomorphic HEMTs studied

We show evidence of the dynamics of trapping centers effects and self-heating of the lattice versus HEMT temperature and biases.

Experimental conditions

For each transistor and at each temperature, DC characterization is achieved to obtain the main extrinsic parameters. Pulsed I-V measurements with 2ns rise time of gate and drain biases allow to follow the evolution of HEMT drain current beyond 10ns pulse length up to several hundredth μ s.

An original cryogenic coplanar probe station coupled with a HP8510C network analyser gives accurate HF measurements up to 40GHz with in-situ calibration and allows the determination of all the access elements of the measured device at each temperature [1].

At each temperature, from 350K down to 10K, a SOLT calibration is achieved in order to make reliable measurements.

A. Light Illumination

One has to note that all our measurements are made under constant illumination to minimize the effects of DX centers. At 300K, no difference can be observed between I-V characteristics in darkness and under light illumination. The current contribution of electron/hole pairs generated by light seems to remain very small versus the main intrinsic Ids current of the HEMT. If holes were generated, part of them at 300K would shift towards the gate and enhance the gate current as it is observed in impact ionization regime. Here there is no change in the gate current in the dark or under illumination. The main interest of the low voltage halogen white light used is to detrapp the electrons from the DX centers. At low temperature, the light modifies obviously the occupation number of surface traps; on the 80nm thick cap layers the effect is negligible but in the recess between the gate edge and the end of the recess, the evolution of the surface potential could influence the device behavior. This distance is smaller than 50nm and under 1.5V drain bias is largely depleted but modelisation should help to better understand this phenomenon.

As far as DX centers are concerned we may notice that DC and HF performances are badly damaged in dark for Vds voltage above 0.8V[6]. There are different ways for trapping electrons in DX centers. The first one under the gate is due to the relative position of the δ -doping well versus the Fermi level for positive gate bias and to lateral diffusion from source access where electron density is very high. The second phenomenon to trap electrons takes place in the drain access region, under the cap layers. Due to the very wide and highly doped GaAs layers there are many electrons in the AlGaAs layer. In both cases, under high field regime ($V_{ds} > V_{dsat}$) they may get enough energy to be trapped by deep level. The last process is very closed to the previous one, electrons which transfer spatially from the channel may be trapped too. This last phenomenon is all the more important than the Vds bias is high.

B. Bias Conditions

The HEMT parameters are determined in several ways. The I-V measurements are performed in DC or in pulsed regime. In both cases the measured parameters are extrinsic and include parasitic access resistances. Pulsed measurements have been used yet to stress both trapping effect [2] and self heating [3] in very small FETs. The time range used is often 200ns-1ms gate or drain pulse. Thanks to the very small intrinsic capacitances of the devices we achieve measurement from a few ns up to 500 μ s. In pulsed regime a few ns after the lead edge, the average HEMT temperature is still near the sample holder temperature and few carriers have been trapped, so the parameter reaches an ideal value more in agreement with results of simulations [4], [5].

The bias condition in HF measurements fixes the population rate of traps and the average temperature of the lattice. The small HF signal power is extremely low and the frequency signal is so high that it does not influence the equilibrium condition imposed by the DC bias point.

Results and discussion

There is no important detrimental short channel effects in the present devices. At each temperature, the threshold voltage shift in current saturation regime is 300mV between $L_g=0.4\mu$ m and $L_g=0.1\mu$ m. Such a threshold voltage shift is relatively moderated if we compare with standard AlGaAs/GaAs HEMTs with same gate lengths. This results from the effect of the heterojunction barrier between the channel and the substrate and from the large aspect ratio which is approximatively equal to 5 at $L_g=0.1\mu$ m. A small reduction in the maximum intrinsic transconductance is obtained for the shortest gatelength ($L_g=0.1\mu$ m and $L_g=0.2\mu$ m), which is probably due to a slightly reduction of the recess depth during the wet etching process.

Fig. 2 shows I-V characteristics of a 0.1μ m gate length HEMT at 50K. It reveals a high current density in the channel due to small distance between gate and channel, high doping in the AlGaAs layer and good quality of the layers.

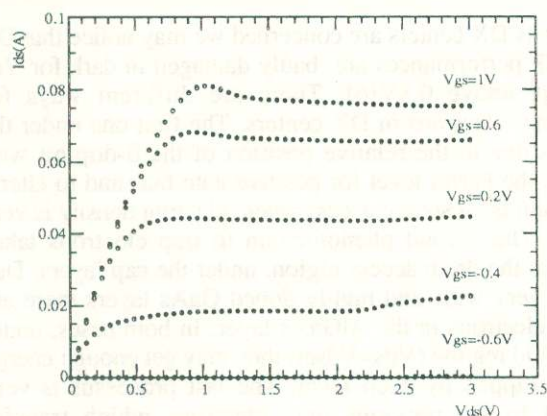


Fig.2 : I-V characteristics of a 0.1μ m* 100μ m gate area at 50K.

The HF output conductance, G_d , : ($G_d=30$ mS/mm for $L_g=0.4\mu$ m) increases slightly at smaller L_g , but remains low ($G_d=34$ mS/mm for $L_g=0.1\mu$ m). This shows that substrate current contribution remains small in such an ultrashort PM-HEMT under moderated V_{ds} bias.

Evolutions of HF G_d versus V_{ds} for a 0.4μ m gate length HEMT at two temperatures $T=300$ K and $T=60$ K are shown on Fig.3. The increase of G_d when cooling down results from transport properties improvement under the gate. Thus, the spatial transfer increases at the end of the gate and the influence of drain voltage on electrons density under the gate increases. A similar behavior is observed when the gate length is reduced.

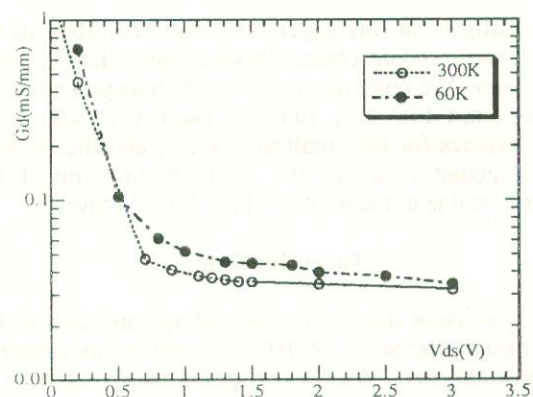


Fig.3 Output conductance of a 0.4μ m gatelength HEMT versus V_{ds} at $T=300$ K and 60K

In order to illustrate the differences between the same parameter measured in different ways we give in table 1 the output conductance at 300K of a $0.1*100\mu$ m² gate area transistor.

The G_d calculated from pulsed measurements does not include self heating and trapping effects (under the cap layers area). Then, it is larger than the two others.

In DC characteristics the time step between two successive V_{ds} points is larger than the thermal equilibrium time and the time capture of the deep centers. So these points do not correspond to the same equilibrium state and this affects the apparent output conductance.

The HF G_d includes trapping effect and self heating due to the bias point but the electron density and the lattice temperature remains in a steady state.

Table 1. : Output conductances of a 0.1μ m* 100μ m HEMT at $V_{gs}=0.4$ V and $V_{ds}=1.5$ V. DC and Pulsed measurements are corrected by the $1-R_sG_m$ factor.

	HF	Pulsed	DC
G_d (ms)	3.4	4.3	2.8

One underlines the relative degradation of transport properties which is observed in the 1-3V drain bias voltage range. It is due to the moderate screening of electrons under the gate from the drain bias in the current saturation

regime, to spatial transfer at the end of the gate and also to the self heating of the lattice. At higher drain voltage ($V_{ds} > 4.5V$) the effect of impact ionization appears.

Fig. 4 compares pulsed I-V measurements : the drain current I_{ds} is shown 5ns after the beginning of the drain pulse and when a steady state is reached. The reduction of I_{ds} versus time is explained by the trapping centers effect and by the increase of lattice temperature in the device and more particularly in the channel.

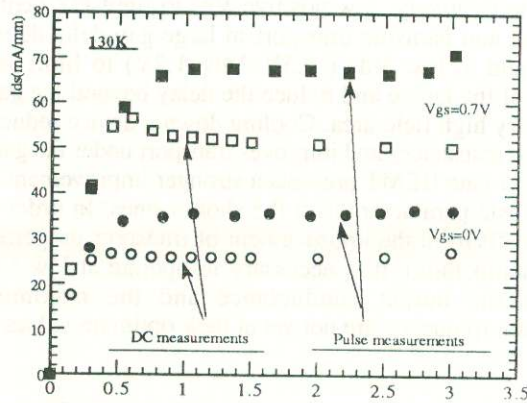


Fig.4: I-V characteristics of a 100nm gatelength HEMT in DC and pulsed regimes.

A clear agreement is obtained for $V_{ds} < 0.4V$ ($V_{gs} = 0V$) and $V_{ds} < 0.6V$ ($V_{gs} = 0.7V$). The discrepancy threshold in V_{ds} between DC and pulsed measurements is temperature dependent and is higher for longer gatelength. The current decrease just above this threshold is due to DX centers trapping while the apparent negative output conductance clearly visible above 1.2V ($V_{gs} = 0.7V$) can be related to self heating. For such a small transistor the very high electric field at the end of the gate and in the drain access and the very high current density allow to reach a very high power density locally in the channel. Of course, with pulsed measurements in the nanosecond-microsecond range time we do not investigate the transient in local temperature regime but the average temperature distribution regime along the whole device.

The high frequency performances versus DC bias conditions are presented in Fig. 1-4 in terms of unity current gain cut off frequencies F_t versus V_{ds} for $L_g = 0.1\mu m$ and $L_g = 0.4\mu m$, and temperatures $T = 300K$ and $60K$. F_t increases steadily when L_g is reduced but its evolution with temperature depends on the gate length.

F_t : Measured value from S-parameters

$$F_{tc} = \frac{G_{mo}}{2\pi(C_{gsint} + C_{gdint} + C_{gselec} + C_{gdelec})}$$

$$F_{ti} = \frac{G_{mo}}{2\pi(C_{gsint} + C_{gdint})}$$

C_{gsint} and C_{gdint} , are intrinsic gate source and gate drain capacitances and G_{mo} the intrinsic transconductance. All these parameters are obtained from small signal equivalent circuit

C_{gselec} and C_{gdelec} are electrostatic parasitic capacitances obtained from finite element calculation and confirmed by careful inspection of small signal equivalent circuit at specific bias [8].

The extrinsic F_t (containing all the resistive and capacitive parasitics) increases at all gate lengths in a similar way upon cooling. The difference between F_t and F_{tc} corresponds to access resistances, degradations. It strongly reduces at low temperature for all the gate length as the access resistances R_s and R_d , decrease by 30% between 300K and 60K. On the other side, the intrinsic F_{ti} increases versus temperature by more than 25% for $L_g = 0.4\mu m$, and only by a few percent for the smaller devices. The intrinsic transconductance G_m presents the same variation as F_{ti}

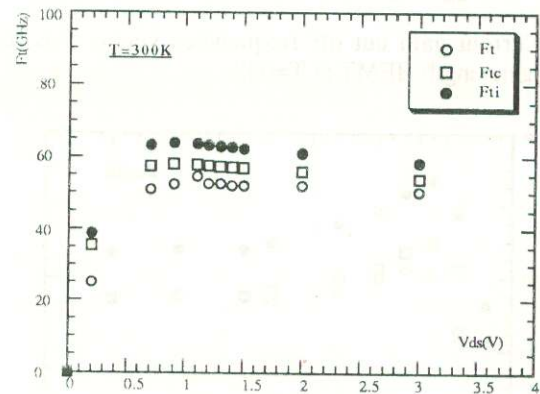


Fig.5 : Current gain cut off frequencies versus V_{ds} for a $0.4\mu m$ gatelength HEMT at $T = 300K$

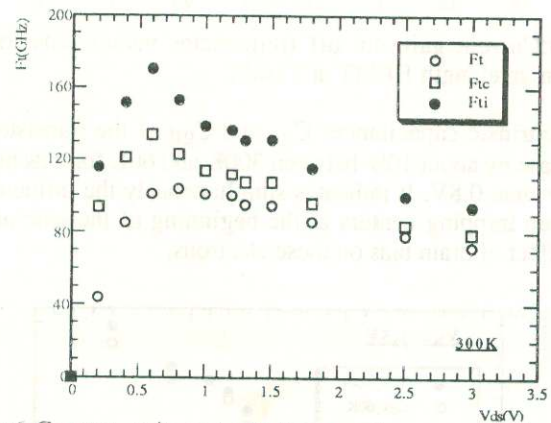


Fig.6: Current gain cut off frequencies versus V_{ds} for a $0.1\mu m$ gatelength HEMT at $T = 300K$

The intrinsic transport properties of the layers (low field mobility, μ_0 and high field velocity) both improve when cooling down. μ_0 increases from $6000cm^2/Vs$ up to $35000cm^2/Vs$ between 300K and 77K [7] and steady state velocity for 50KV/cm electrical field increases at least 50% [9]. The F_t decrease at high V_{ds} voltage always well correlated with the I_{ds} decrease linked to trapping and self heating observed in I-V DC curves. This effect occurs at lower V_{ds} bias for the shorter gatelength HEMTs and may explain the apparent saturation of HF performance at low temperature; while the F_{ti} improvement for the longer

gatelength devices is probably a signature of ballistic effect at low temperature.

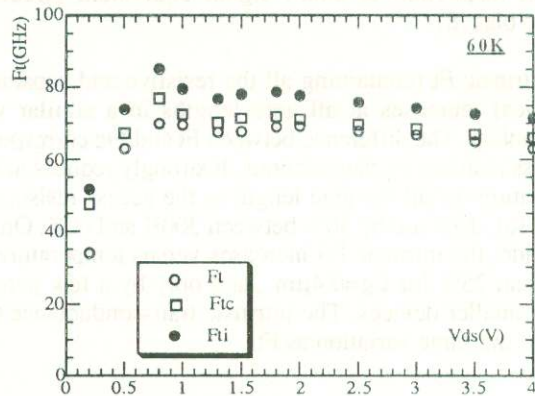


Fig.7:Current gain cut off frequencies versus V_{ds} for a $0.4\mu\text{m}$ gatelength HEMT at $T=60\text{K}$

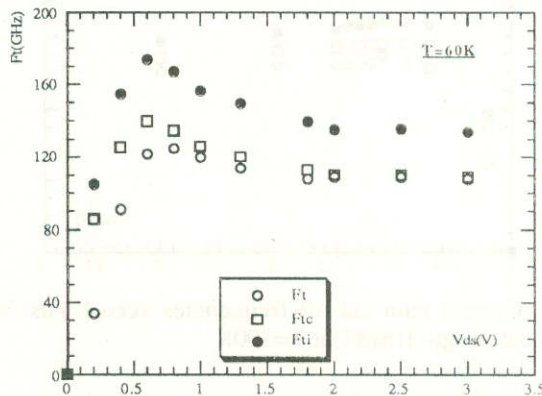


Fig.8:Current gain cut off frequencies versus V_{ds} for a $0.1\mu\text{m}$ gatelength HEMT at $T=60\text{K}$

The intrinsic capacitances C_{gs} and C_{gd} of the transistors decrease by about 10% between 300K and 60K for V_{ds} bias larger than 0.8V. It indicates simultaneously the influence of deep trapping centers at the beginning of the gate and the effect of drain bias on these electrons.

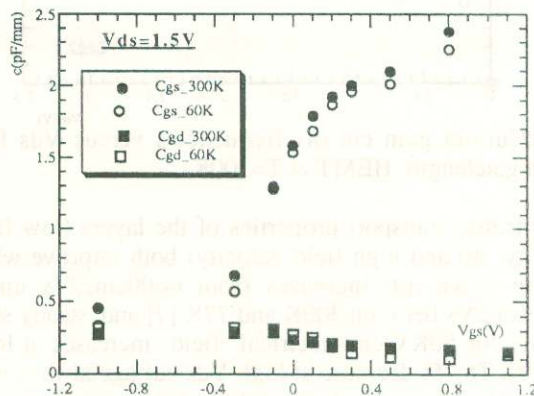


Fig. 9. C_{gs} and C_{gd} capacitances versus V_{gs} at $V_{ds}=1.5\text{V}$ for $T=300\text{K}$ and 60K $L_g=0.3\mu\text{m}$

Theses result are consistent with the above results.

Self consistent simulations of Poisson and Schrödinger equations along the growth axis confirm that the population under the gate is nearly identical at 60K and 300K when the channel is fully opened and the deep level of the DX centers is neglected

Conclusion

The overall dc, pulsed and HF measurements show that a good trade off for best HF performances is to operate PM-HEMT at relatively low positive V_{gs} to limit DX center influence and parasitic transport in large gap delta doped layers, and at low V_{ds} ($0.5\text{V} < V_{ds} < 1.2\text{V}$) to limit self heating of the lattice and reduce the delay beyond the gate in the very high field area. Cooling down a device reduces all access resistances and improves transport under the gate. The larger gate HEMT presents a stronger improvement of the intrinsic parameters than the shorter ones. In order to take benefit from the improvement of transport properties at low temperature it is necessary to operate at low V_{ds} even if the output conductance and the maximum oscillation frequency are not yet at their optimum values.

(*) The authors are indebted to Dr. Linh and Dr. Rochette from Picogiga for the epitaxial layers.

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